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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,250	12/20/2000	Carl Werner	60809-5069-US	8064

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/742,250	WERNER ET AL.
	Examiner	Art Unit
	Linh V. Nguyen	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20* is/are allowed.

6)☒ Claim(s) *1-3,5,6,9 and 10* is/are rejected.

7)☒ Claim(s) *7,8 and 21-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's communication filed on 2/26/06. Claim 4 has been canceled. Claims 1, 5 and 21 have been amended. Claims 1 – 3 and 5 - 23 are pending on this office action.

Response to Arguments

2. Applicant's arguments, with respect to amended claim 1 have been fully but they are not persuasive, because each transistors (S3's) in the current mode driver (L1 – L255) is corresponding to each bit (Fig.6 [D1 – D255]), and the control signal providing correction for multiples L1 – L255 (Col. 8 lines 1 – 15; lines 31 – 36); therefore, the control signal (output of 34) must includes multiple bits in order performing correction of all L1 – L255 for all D1 – D255 inputs of DA converter 11.

Per explained above, Koyama et al. from previous office action is applying to this office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 3, and 15 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. U.S. Patent No. 5,703,582.

Regarding claim 1, Fig. 1 of Koyama et al. discloses a method for improving resolution of a current driver, where the current mode driver (Fig. 1) is operable to provide an output that falls within a predetermined range (Col. 4 lines 44 – 54), the method comprising the steps of: sensing (34) at least one of a process condition, a voltage condition and a temperature condition (Col. 6 lines 7 - 13) with a PVT detector (34); adjusting a full scale current of a DAC (Col. 9 lines 10 - 15) in accordance with an output of the PVT detector (output of 34) ; and setting a current control signal (control gates of S3s) based on an output of the DAC (41, 42), the current control signal (control gates of S3s) being applied to the current mode driver (S3) to improve resolution of the current mode driver (Fig. 1; also see Fig. 6); wherein the current control signal (output of 34) for transistors (S3's) in current mode driver (L1 – L255) comprises a plurality of bits (See explained above, under response to arguments).

Regarding claim 2, wherein the step of adjusting the full-scale current comprises the steps of: generating an adjustment signal (output of 34) in response to the sensing steps (34); and applying the adjustment signal to the current mode driver (S3), the adjustment signal causing the current mode driver (Fig. 1; also see Fig. 6) to adjust the full scale current (Col. 9 lines 10 - 15).

Regarding claim 3, wherein the step of applying the adjustment signal (output of 34) to the current mode driver (S3) comprises applying at least one predetermined voltage (output of 34) to a corresponding at leas one transistor switch (S3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. as applied to claim 1 above, in view of Gillig U.S. patent No. 5,604,468.

Koyama et al. as applied to claim 1 above, discloses the sensing step (34) in a lock-loop condition. However, Koyama et al. does not explicitly disclose the lock-loop is either a delay lock loop or phase lock loop.

Fig. 5 Gillig teaches a temperature-sensing system comprises determining a condition associated with a phase-locked loop or a delayed-locked loop (Col. 4 line 62 - Col. 5 line 10).

Koyama et al. Gillig are common subject matter of sensing circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the locked-loop circuit taught by Gillig's sensing-circuit to the sensing-circuit of King et al. for the purpose of providing accurate, linear and repeatable temperature compensation with more simplified circuitry (Gillig' s Col. 2 lines 1 - 4).

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. as applied to claim 1 above.

Regarding claim s 9 and 10, Koyama et al. as applied to claim 1 above, does not explicitly disclose the sensitive parameter (output of 34) is either in the form of AC or DC parameter. However, AC or DC sensitive parameter is clearly a desire of interests as indicated by applicant claims 9 and 10. Therefore, it would have been obvious to one in the art at the time the invention was made to implement the sensitive element of Koyama et al. in either in the form AC or DC parameter for desire of interests, which has indicated by applicant on claims 9 and 10 above.

Allowable Subject Matter

8. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest applying a PVT independent current to a PVT sensitive load; and detecting a voltage drop across the PVT sensitive load.

9. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest applying a pulse in parallel to a delay line and a first plurality of latches, wherein the delay lines comprises a second plurality of delay stages; coupling an output of a subset of the plurality of delays stages to an input of a corresponding latch.

10. Claim 21 –23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. With respect to claim 21, prior art does not teach or suggest the multi-PAM signal generator uses pulses having a plurality of sets of signal amplitudes to encode signals, and wherein a respective set of signal amplitudes in the plurality of sets of signal amplitudes has at least tow signal levels.

11. Claims 11 - 14 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 11, in addition to other elements in the claim, the prior art doest not teach or suggest a current output driver having: applying the current control signal to cause the output driver to sink a second current; wherein the second current is less than the full scale current; and applying a second current adjustment signal to alter the second current pf the output driver; and calibrating the altered full scale current of the output driver and the altered second current of the output driver by comparing the altered full scale current with a first reference and comparing the altered second current with a second reference.

12. Claims 15 - 20 are allowed.

With respect to claim 15, in addition to other element in the claim the prior art does not teach or suggest a current mode driver, comprising the steps of: applying the first output as a gate voltage to control a full scale current of an output driver DAC calibrating the output driver by comparing a second output, which is provided by the output driver, with a reference ; and augmenting the first current control signal when the second output differs from the reference.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Conclusion

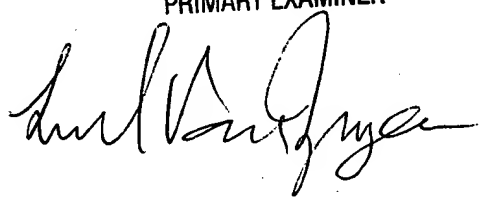
14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

LINH NGUYEN
PRIMARY EXAMINER



4/14/06

Linh Van Nguyen

Art Unit 2819